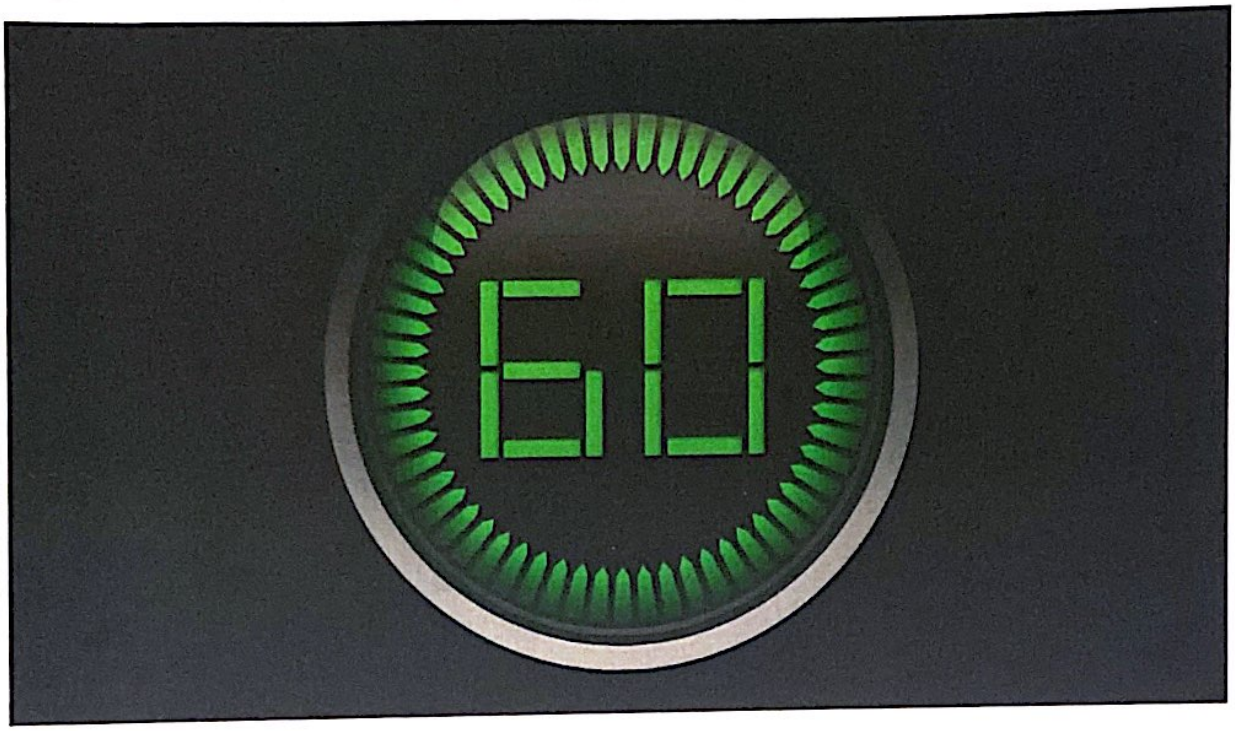
Sixty Second Timer



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Introduction

In this project, students have the opportunity to draw all of the concepts and skills that students have developed pertaining to this topic. The students will design, simulate and create a sixty-second timer. A circuit that counts from zero to 60. Some of the skills students learned during this project were, working with breadboard, computer simulated circuits, and AOI logic. The skills students will learn is working with synchronous counter (MSI, SSI), multiplexer and programming.

Design Brief

Client – Track team

Designer – Keyur Rana

Design Statement – You will design, simulate and create a sixty-second timer

Constraints –

- The two output displays are common cathode 7 segment display that you will require a multiplex signal
- Each display will use a 74Ls48 BCD-to seven segment display driver in design mode (DEC-BCD-7)'
- A synchronous counter designed with a 74LS163 MSI counter IC (CNTR-4BIN-S) controls the ones-unit display (0-9).
- The tens-unit display (0-6) is controlled by an synchronous counter designed with SSI logic gates (J/K)
- Any additional logic may be used as needed to support the counter designs.

Deliverables –

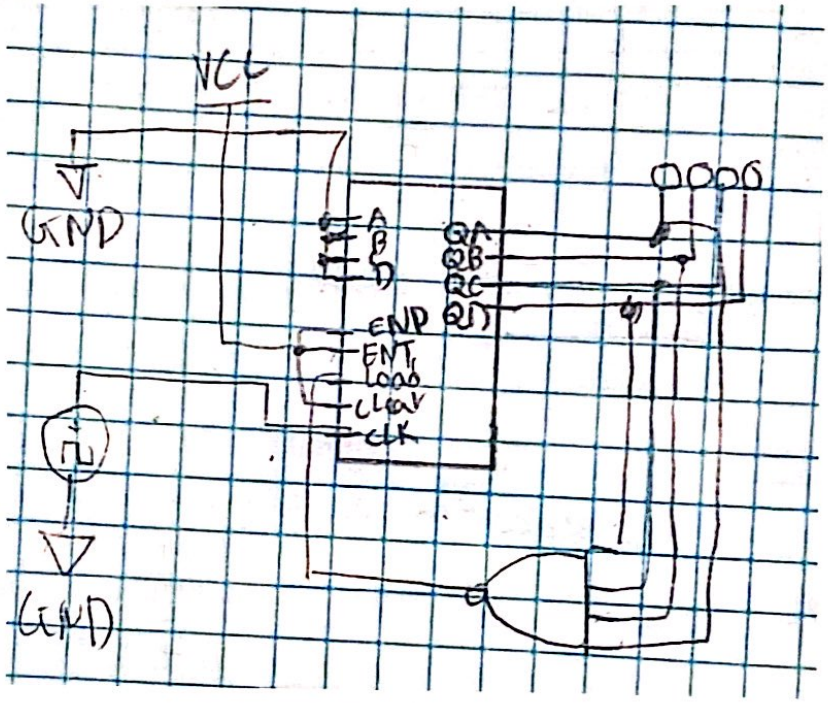
- AOI and NAND – NOR Logic
- Multisim

Materials

Description	Quantity	Part #
Multism	1	14.1
Wires	-	-
Breadboard	1	800949B-01
FPGA	1	CMOD S6
myDAQ	1	-

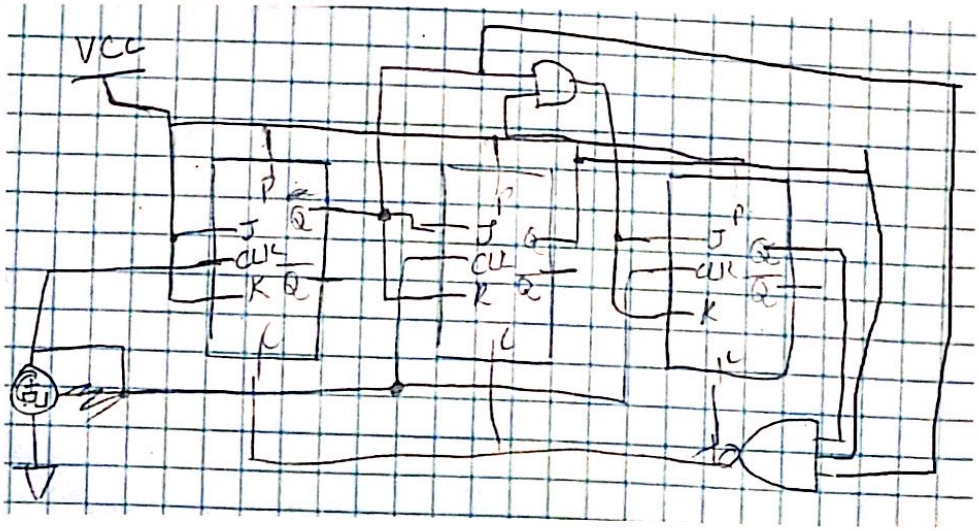
Evidence of Working Design – Hand drawn completed Circuit

One's place -



MSI

Ten's place –

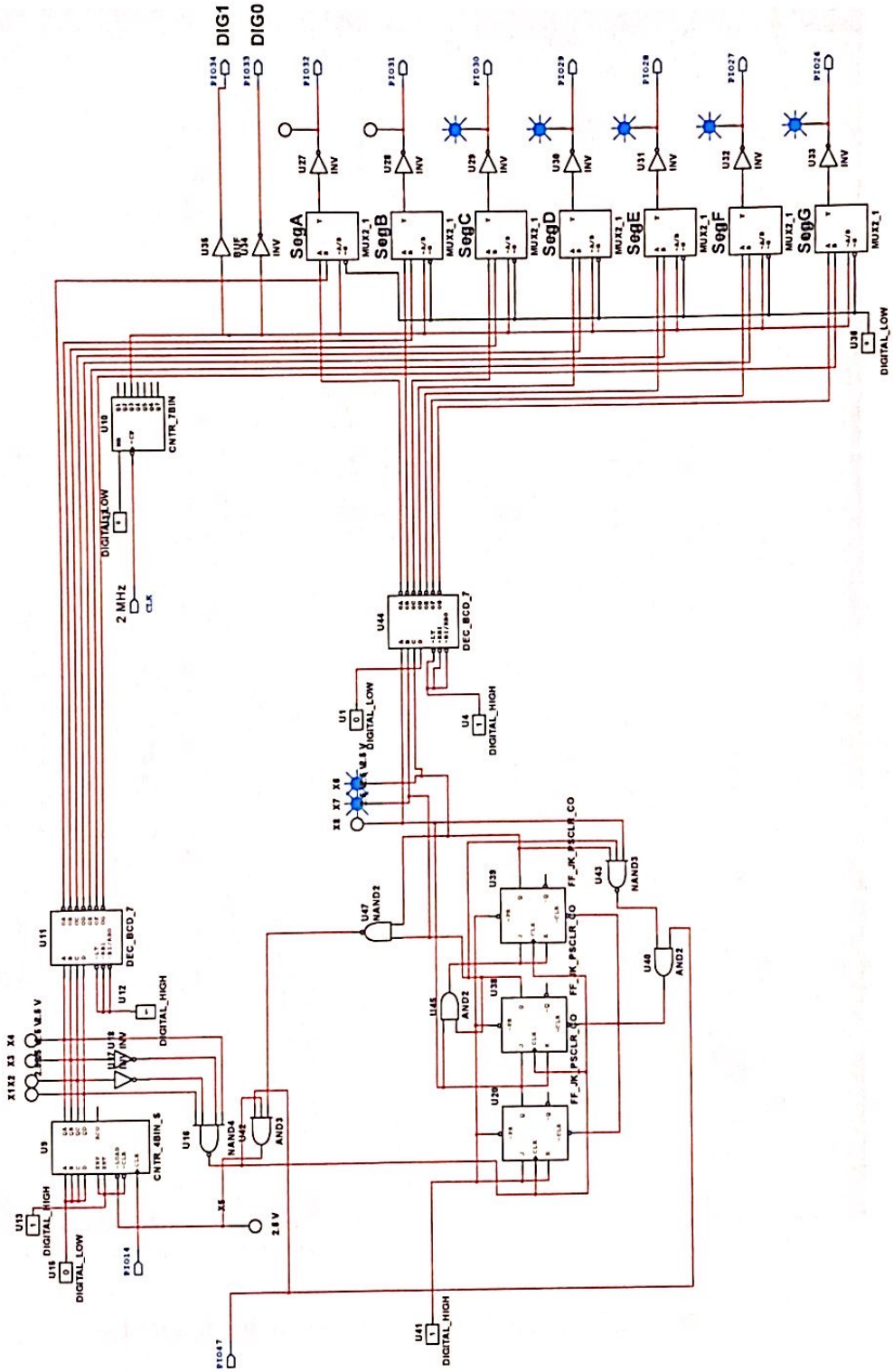


The hand drawn circuits in the Engineering Notebook (SSI)

Evidence of Working Design – Computer Simulated Circuit

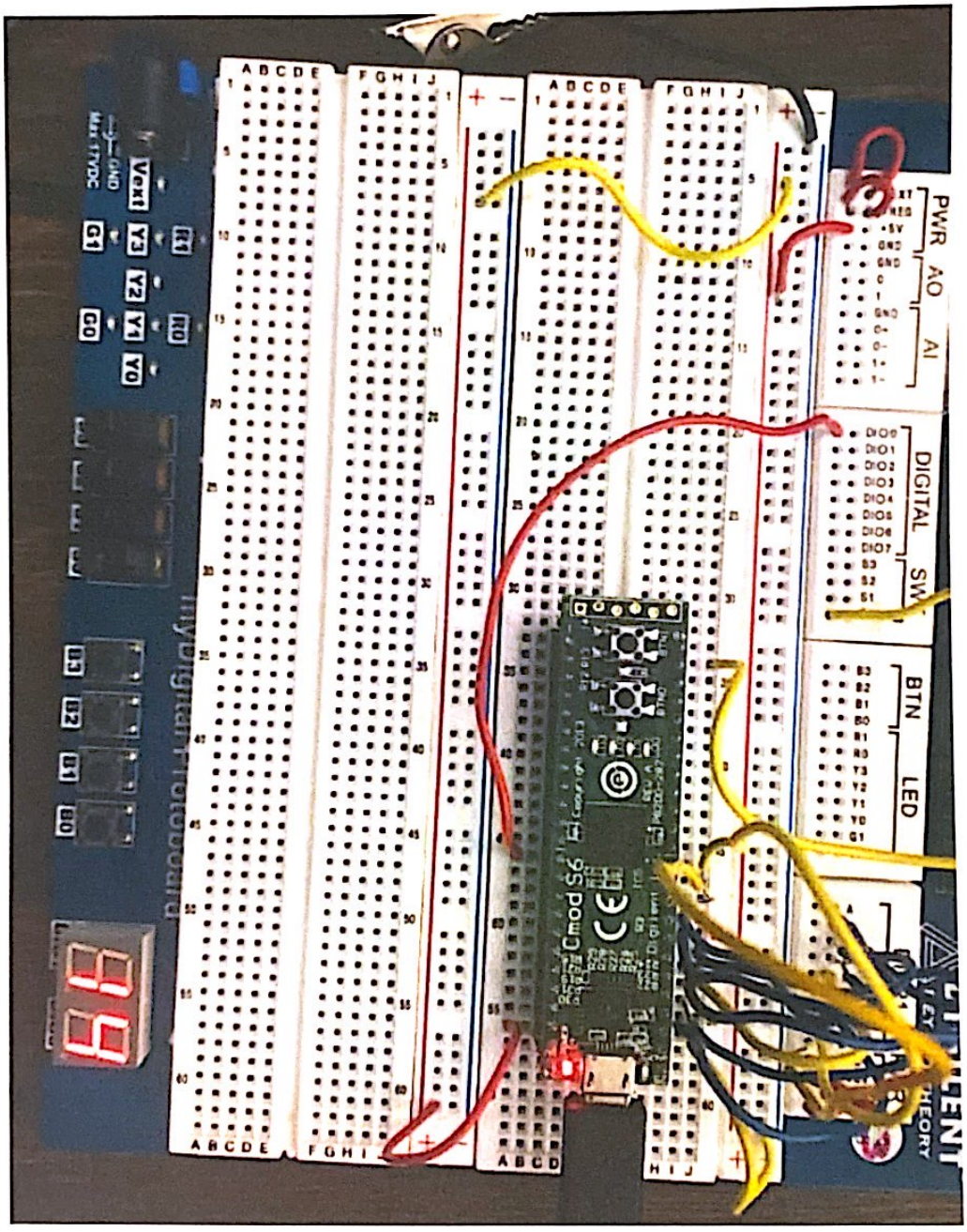
DIG 1 = Connect B inputs of the 2 to 1 MUX to create the number 8

DIG 0 = Connect A inputs of the 2 to 1 MUX to create the number 4



This is the Sixty Second Timer build on Multisim in PLD mode

Evidence of Working Design – Program Circuit



The working sixty-second timer on the breadboard

Conclusion

In this project, skills that students will learn from this project is working with synchronous counter (MSI, SSI), multiplexer and programming. The students will design, simulate and create a sixty-second timer. A circuit that counts from 00 to 60. Some of the skills students learned during this project were, working with breadboard, computer simulated circuits, and AOI logic. The steps students took to complete this project was similar to the previous project that involved counting from 00-80. Instead, it was from 00-60. Students started by designing the circuit in their engineering notebook and then creating the two circuits, 74LS163 MSI counter that counted from 0-9 and J/K synchronous that counted from 0-6 on Multisim PLD mode. Next, they connected it using AOI logic gates. The challenges were to make the circuit count from 00 to 60. Stop at 60 and manually reset it with a switch. During this process, the students had many difficulties overcoming these obstacles. At the end, they managed to get their circuit working on the PLD mode. They attached a seven-segment driver to the two counters and hooked it up with an 84 circuit from the previous project. During the time of programming, students faced many more obstacles. For example, when programming, the seven segments drivers were accidently detached from the 84 circuit that caused errors transferring. Another common was when leaving the digital clock attached to the circuit in PLD mode; it caused the circuits to only count from 00-40. It's not true if other students had this problem, but personally, I had this and it was a struggle overcoming it because I couldn't debug the cause of the circuit on breadboard only counting from 00-40 when it worked completely

fine on the PLD mode. Overall, this project was very small and interesting. I would love to do these kinds of project in the near project.